

WHAT IS CLAIMED IS:

1. A ferroelectric memory comprising:

a passive matrix array in which memory cells formed of

5 ferroelectric capacitors are arranged; and

a peripheral circuit for the passive matrix array,

wherein:

the passive matrix array is formed on a microstructure;

the peripheral circuit is formed on a substrate; and

10 the microstructure is integrated on the substrate.

2. A ferroelectric memory comprising:

a passive matrix array in which memory cells formed of
ferroelectric capacitors are arranged; and

15 a peripheral circuit for the passive matrix array,
wherein:

the passive matrix array is formed on a substrate;

the peripheral circuit is formed on a microstructure; and

the microstructures is integrated on the substrate.

20 3. A ferroelectric memory comprising:

a passive matrix array in which memory cells formed of
ferroelectric capacitors are arranged; and

a peripheral circuit for the passive matrix array,

25 wherein:

the passive matrix array is formed on a first
microstructure;

the peripheral circuit is formed on a second microstructure; and

the first and second microstructures are integrated on a substrate.

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4. The ferroelectric memory according to claim 1, 2, or 3, wherein a plurality of microstructures is integrated in the case where the passive matrix array is formed on the microstructure, and a plurality of microstructures is integrated in the case
10 where the peripheral circuits are formed on the microstructures.

5. The ferroelectric memory as defined in any one of claims 1 to 4, wherein:

15 a recess portion in which the microstructure is provided is formed in the substrate; and

the microstructure is provided in the recess portion and integrated on the substrate.

20 6. The ferroelectric memory as defined in claim 5, wherein the substrate is formed by transfer-molding a photocurable resin.

7. A ferroelectric memory comprising:

25 a passive matrix array in which memory cells formed of ferroelectric capacitors are arranged;

a peripheral circuit for the passive matrix array; and

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a plurality of pairs of the passive matrix array formed on a first microstructure and the peripheral circuit formed on a second microstructure,

wherein at least one of the pairs is provided on each side of a substrate.

8. A ferroelectric memory comprising:

a passive matrix array in which memory cells formed of ferroelectric capacitors are arranged;

a peripheral circuit for the passive matrix array; and
an associated circuit having the same function as the ferroelectric memory or a different function from the ferroelectric memory, wherein:

the passive matrix array, the peripheral circuit and the associated circuit are formed on each of a plurality of microstructures; and

the microstructures are integrated on a single substrate.

9. A ferroelectric memory comprising:

a passive matrix array in which memory cells formed of ferroelectric capacitors are arranged; and

a peripheral circuit for the passive matrix array,
wherein the passive matrix array and the peripheral circuit are integrated on a single microstructure.

10. A ferroelectric memory comprising:

a passive matrix array in which memory cells formed of

ferroelectric capacitors are arranged; and

a peripheral circuit for the passive matrix array,
wherein:

the passive matrix array is formed on a first
5 microstructure;

the peripheral circuit is formed on a second
microstructure which is larger than the first microstructure;
and

the first microstructure is provided in a part of the
10 second microstructure to be integrated.

11. A ferroelectric memory comprising:

a passive matrix array in which memory cells formed of
ferroelectric capacitors are arranged; and

15 a peripheral circuit for the passive matrix array,
wherein:

the passive matrix array is formed on each of a plurality
of microstructures; and

the microstructures are provided in layers to be
20 integrated in a substrate.

12. A method of fabricating a ferroelectric memory which
includes: a passive matrix array in which memory cells formed
of ferroelectric capacitors are arranged; and a peripheral
25 circuit for the passive matrix array, wherein:

the passive matrix array is formed on a microstructure;
the peripheral circuit is formed on a substrate; and

the microstructure is integrated on the substrate.

13. A method of fabricating a ferroelectric memory which includes: a passive matrix array in which memory cells formed of ferroelectric capacitors are arranged; and a peripheral circuit for the passive matrix array, wherein:

the passive matrix array is formed on a substrate;
the peripheral circuit is formed on a microstructure; and
the microstructure is integrated on the substrate.

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14. A method of fabricating a ferroelectric memory which includes: a passive matrix array in which memory cells formed of ferroelectric capacitors are arranged; and a peripheral circuit for the passive matrix array, wherein:

15 the passive matrix array is formed on a first microstructure;

the peripheral circuit is formed on a second microstructure; and

the first and second microstructures are integrated on
20 a substrate.

15. The method of fabricating a ferroelectric memory as defined in any one of claims 12 to 14, wherein:

a substrate having a recess portion which corresponds to
25 a shape of the microstructure is provided; and

the microstructure is provided in the corresponding recess portion in the substrate to be integrated.

16. The method of fabricating a ferroelectric memory as defined in claim 15,

wherein the microstructure is provided in the recess
5 portion in the substrate by providing a fluid which contains the microstructure to a surface of the substrate.

17. A method of fabricating a ferroelectric memory which includes: a passive matrix array in which memory cells formed
10 of ferroelectric capacitors are arranged; and a peripheral circuit for the passive matrix array, wherein:

a plurality of pairs of the passive matrix array formed on a first microstructure and the peripheral circuit formed on a second microstructure are provided: and

15 at least one of the pairs is integrated on each side of a substrate.

18. A method of fabricating a ferroelectric memory, which includes: a passive matrix array in which memory cells formed
20 of ferroelectric capacitors are arranged; and a peripheral circuit for the passive matrix array, wherein:

the passive matrix array is formed on a first microstructure;

the peripheral circuit is formed on a second
25 microstructure which is larger than the first microstructure; and

the first microstructure is provided in a part of the

second microstructure to be integrated.

19. A method of fabricating a ferroelectric memory, which includes: a passive matrix array in which memory cells formed
5 of ferroelectric capacitors are arranged; and a peripheral circuit for the passive matrix array, wherein:

the passive matrix array is formed on each of a plurality of microstructures; and

the microstructures are provided in layers to be
10 integrated in a substrate.

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